Amendments to the Claims:

Please amend the claim as follows in a complete set of the claims.

Claims (complete set).

1. (Currently amended) A chip comprising:

a transmitter including a cycle encoding circuit to receive a data input signal and to provide a full cycle encoded signal in response thereto by continuously joining portions of different encoding signals, wherein some of the encoding signals have a different frequency than others of the encoding signals and some of the encoding signals have a different phase than others of the encoding signals, and wherein data is represented in data time segments of the full cycle encoded signal and no data time segment has more than one cycle of an encoding signal;

wherein each of the data time segments have the same time duration; and

wherein the cycle encoding circuit includes a multiplexer to receive the data input signal and the encoding signals and to select the portions of the encoding signals that are to form the full cycle encoded signal in response to the data input signal.

2. (Original) The chip of claim 1, wherein the transmitter further includes a complementary cycle encoding circuit to receive the data input signal and to provide a complementary full cycle encoded signal in response thereto.

3. (Currently amended) The chip of claim 1, wherein the multiplexer is to select the portions of the encoding signals that are to form the full cycle encoded signal in response to which encoding signal was selected for a previous data time segment.

4. (Original) The chip of claim 1, further comprising a periodic signal source to provide a periodic reference signal and wherein the transmitter includes circuits to provide the encoding signals in response to the periodic reference signal.

5. (Original) The chip of claim 4, wherein the periodic reference signal has period that is equal to the time length of the data time segments.

6. (Original) The chip of claim 4, wherein the periodic reference signal has a period that is equal to the time length of a data bit cell of the data input signal.

7. (Original) The chip of claim 1, wherein the encoding signals include a first signal with frequency F, a second signal that is an inverse of the first signal, a third signal that has a frequency F/2, and a fourth signal that is an inverse of the third signal.

8. (Original) The chip of claim 1, wherein the full cycle encoded signal represents a 0 or a 1 depending on the value of the data.

9. (Previously presented) The chip of claim 1, further comprising a receiver that includes an initial receiving circuit to receive the full cycle encoded signal, a delay circuit to delay at least one signal provided by the initial receiving circuit, and a logic circuit to receive at least one signal from the delay circuit and in response thereto to provide a data out signal which includes recovered data from the full cycle encoded signal.

10. (Currently amended) A chip comprising:

a transmitter including a cycle encoding circuit to receive a data input signal and a periodic reference signal and to provide a cycle encoded signal in response thereto, wherein in response to the data input signal and the periodic reference signal, the cycle encoded signal is formed of continuously joined portions of encoding signals during successive data time segments, wherein some of the encoding signals have a different frequency than others of the encoding signals and some of the encoding signals have a different phase than others of the encoding signals;

wherein each of the data time segments have the same time duration;

wherein the transmitter further includes a complementary cycle encoding circuit to receive the data input signal and the periodic reference signal and to provide a complementary cycle encoded signal in response thereto, wherein the complementary cycle encoded signal is a logical inverse of the cycle encoded signal; and

wherein the cycle encoding circuit includes a multiplexer to receive the data input signal and the encoding signals and to select the portions of the encoding signals that are to form the full cycle encoded signal in response to the data input signal.

11. (Original) The chip of claim 10, wherein the cycle encoded signal is a full cycle encoded signal in which no data time segment has more than one cycle of an encoding signal.

12. (Canceled)

13. (Original) The chip of claim 10, wherein the cycle encoding circuit includes a multiplexer to receive the data input signal and the encoding signals and to select the portions of the encoding signals that are to form the cycle encoded signal in response to the data input signal and which encoding signal was selected for a previous data time segment.

14. (Original) The chip of claim 10, wherein the encoding signals include a first signal with frequency F, a second signal that is an inverse of the first signal, a third signal that has a frequency F/2, and a fourth signal that is an inverse of the third signal.

15. (Currently amended) The chip of claim 10, further comprising a receiver that includes an initial receiving circuit to receive the ~~full~~ cycle encoded signal and complementary cycle encoded signal, a delay circuit to delay at least one signal provided by the initial receiving circuit, and a logic circuit to receive at least one signal from the delay circuit and in response thereto to provide a data out signal which includes recovered data from the ~~full~~ cycle encoded signal.

16. (Currently amended) A system comprising:

a transmitter including a cycle encoding circuit to receive a data input signal and to provide a full cycle encoded signal in response thereto by continuously joining portions of different encoding signals, wherein some of the encoding signals have a different frequency than others of the encoding signals and some of the encoding signals have a different phase than others of the encoding signals, and wherein data is represented in data time segments of the full cycle encoded signal and no data time segment has more than one cycle of an encoding signal; and

a receiver to receive the full cycle encoded signal and recover values of the data input signal in response thereto, wherein the receiver includes an initial receiving circuit to receive the full cycle encoded signal, a delay circuit to delay at least one signal provided by the initial receiving circuit and provide two signals delayed by different amounts and comparison circuitry to compare the two delayed signals, and a logic circuit to receive ~~at least one signal from the delay circuit~~ an output of the comparison circuitry and in response thereto to provide a data out signal which includes recovered data from the full cycle encoded signal.

17. (Original) The system of claim 16, wherein the transmitter further includes a complementary cycle encoding circuit to receive the data input signal and to provide a complementary full cycle encoded signal in response thereto.

18. (Original) The system of claim 16, wherein the cycle encoding circuit includes a multiplexer to receive the data input signal and the encoding signals and to select the portions of the encoding signals that are to form the full cycle encoded signal in response to the data input

signal and which encoding signal was selected for a previous data time segment.

19. (Original) The system of claim 16, further comprising a periodic signal source to provide a periodic reference signal and wherein the transmitter includes circuits to provide the encoding signals in response to the periodic reference signal.

20. (Original) The system of claim 16, wherein the encoding signals include a first signal with frequency F, a second signal that is an inverse of the first signal, a third signal that has a frequency F/2, and a fourth signal that is an inverse of the third signal.

21. (Canceled)

22. (Previously presented) The system of claim 16, wherein the recovered values are the inverse of those of the data input signal.

23. (Currently amended) A system comprising:

a transmitter including:

(a) a cycle encoding circuit to receive a data input signal and to provide a cycle encoded signal in response thereto by continuously joining portions of different encoding signals, wherein some of the encoding signals have a different frequency than others of the encoding signals and some of the encoding signals have a different phase than others of the encoding signals, wherein the cycle encoding circuit includes a multiplexer to receive the data input signal and the encoding signals and to select the portions of the encoding signals that are to form the full cycle encoded signal in response to the data input signal; and

(b) a complementary cycle encoding circuit to receive the data input signal and to provide a complementary cycle encoded signal in response thereto by continuously joining portions of the different encoding signals; and

a receiver to receive the cycle encoded signal and the complementary cycle encoded signal and to recover values of the data input signal in response thereto.

24. (Currently amended) The system of claim 23, wherein data is represented in data time segments of the cycle encoded signal and wherein the cycle encoding circuit includes a multiplexer to receive the data input signal and the encoding signals and to select the portions of the encoding signals that are to form the cycle encoded signal in response to the data input signal and which encoding signal was selected for a previous data time segment.

25. (Original) The system of claim 23, further comprising a periodic signal source to

provide a periodic reference signal and wherein the transmitter includes circuits to provide the encoding signals in response to the periodic reference signal.

26. (Original) The system of claim 23, wherein the encoding signals include a first signal with frequency F, a second signal that is an inverse of the first signal, a third signal that has a frequency F/2, and a fourth signal that is an inverse of the third signal.

27. (Previously presented) The system of claim 23, wherein the receiver includes an initial receiving circuit to receive the full cycle encoded signal, a delay circuit to delay at least one signal provided by the initial receiving circuit, and a logic circuit to receive at least one signal from the delay circuit and in response thereto to provide a data out signal which includes the recovered values of the data input signal.

28. (Currently amended) The system of claim 23, wherein data is represented in data time segments of the cycle encoded signal and wherein the cycle encoded signal is a full cycle encoded signal in which no data time segment has more than one cycle of an encoding signal.